REMARKS

Claims 1, 8, 13, and 18 have been amended to clarify certain features of the Applicant's claimed processor and associated method. Written support for the added features is found in the drawings, in the corresponding text in the specification, and in the original claims. No new matter is added by the amendments.

The Applicant respectfully requests reconsideration of the rejections set forth in the Official Action in view of the amendments to the claims and the following remarks.

35 USC 112, First Paragraph: Claims 1, 3-8, and 10-12

The Examiner rejected Claims 1, 3-8, and 10-12 under 35 USC 112, first paragraph. In making the rejection the Examiner asserted that the term "...sound system processor..." in Claims 1, 3-8 and 10-12 does not have written support in the specification. Claims 1 and 8 have been amended to recite "A *processor* for providing in-line early reflection enhancement in a sound system..." (Emphasis added). Claims 1 and 8 also recite that the processor has "*multiple outputs adapted for outputting the delayed discrete reproductions of the microphone signals to* a number of loudspeakers" (Emphasis added). The processor recited in Claims 1 and 8 is clearly disclosed in Figure 1, and also described, for example, in the last paragraph on page 7 of the present application. Accordingly, it is believed that this ground of rejection has been overcome.

35 USC 112, First Paragraph: Claims 1, 3-8, 10-13, 15-18, and 20

The Examiner rejected Claims 1, 3-8, 10-12, 15-18, and 20 under 35 USC 112, first paragraph. In making the rejection the Examiner asserted that the subject matter of the rejected claims is not supported by an enabling disclosure. More specifically, the

Examiner stated:

> The disclosure discloses the processor, which generates a number of delayed reproductions as shown in Figs. 2, 3, 4, and 5. However, in Fig. 1, the processor outputs only two outputs. Therefore the disclosure does not clearly disclose in the disclosure for one of ordinary skill in the art to make or use the system in order to utilize the number of delayed reproductions to output two output signals from the processor. In this regards [sic], the specification is merely an invitation to experiment, i.e. Applicant is requiring the public to disclose how to make the invention work, as opposed to disclosing it to the public.

Applicant respectfully disagrees with the Examiner's assertion that Figure 1 shows only two outputs for the processor. The processor actually outputs more than two signals, which is clearly shown in Figure 1 of the present application. The processor shown in Figure 1 outputs at least four signals, each of the four signals being output to a respective speaker L_1 to L_k. Figure 1 clearly shows a line extending from each speaker to the processor. It is also noted that the lines from the processor to speakers L_1 and L_3 have been co-joined near the processor for clarity, as have the lines to speakers L_2 and L_k. This does not mean that there are only two outputs from the processor. The Examiner should recognize that Figure 1 is a schematic diagram. It is not a connection diagram. The joining of the lines is a technique used by those skilled in the art to simplify a schematic diagram. The information provided in Figures 1-5 and in the corresponding written description, is sufficient for a person skilled in the art to make and use the Applicant's claimed processor and sound system without undue experimentation.

In view of the foregoing explanation, it is believed that the rejection based on lack of an enabling disclosure is not supported by substantial evidence. Therefore, the rejection is improper and should be withdrawn.

35 USC 102(e): Claims 1, 3-5, 8, 10-13, 15, 18, and 20

The Examiner rejected Claims 1, 3-5, 8, 10-13, 15, 18, and 20 under 35 USC 102(e) as being anticipated by US Patent No. 5,812,674 (Jot et al.). The Applicant respectfully traverses this rejection for the following reasons.

In the response submitted on May 5, 2006, the Applicant presented extensive arguments why Jot et al. does not anticipate the Applicant's claimed invention as set forth in Claims 1 and 8. Those arguments are reiterated here and incorporated in this response. In the Official Action mailed on July 26, 2006 the Examiner responded to those arguments in paragraphs 25-33 of the Official Action.

In paragraph 25, the Examiner refers to the Applicant's previous submission that Jot et al. does not "...describe a sound system processor that has an early reflection stage having a unitary transfer function matrix such that the sound system processor has an overall power gain that is substantially constant with the frequency to improve stability in the sound system". The Examiner disagrees with that argument. The Examiner states that Jot et al. discloses an early reflection stage similar to that of the Applicant's invention shown in Figures 2, 3, 4 and 5. He states that the early reflection stage of Jot et al. comprises: a delay 731, a unitary mixing matrix 741, a delay 742, and a unitary mixing matrix 750 in which the output signals maybe directly reproduced on a loud speaker device. It appears that the Examiner is asserting that the sub-system he refers to does have a unitary transfer function matrix such that the sound system processor has an overall power gain that is substantially constant with the frequency to improve stability in the sound system. However, he does not provide any technical explanation to support that assertion.

The Applicant respectfully maintains his previous position that Jot et al. does not describe a processor that has an early reflection stage that has *a unitary transfer function matrix such that the processor has an overall power gain that is substantially constant with the frequency to improve stability in the sound system.* The combination of components shown and described in Jot et al. and referred to by the Examiner form part of a sub-system path that has one input (Omni) and four "surround" outputs (S1-S4). Applicant submits that this sub-system path in Jot et al. comprising the delay 731, unitary mixing matrix 741, delay 742 and unitary mixing matrix 750 does not provide a unitary transfer function matrix such that the sound system processor has an overall power gain that is substantially constant with the frequency to improve stability in the sound system.

In order to demonstrate the validity of the foregoing arguments, the declaration of the Applicant, Dr. Mark Poletti is submitted with this response. The Poletti declaration provides detailed technical reasons to explain why the system described and shown in Jot et al. does not provide a unitary transfer function matrix as set forth in Claims 1 and 8 of the present application. The Poletti declaration presents a detailed mathematical analysis with respect to Figure 9 of Jot et al. and a matrix equation comprising the multiplication of matrices representing the individual transfer function matrices of individual components in the sub-system path.

The Poletti declaration shows mathematically the overall transfer function matrix for the room module of the Jot et al. system is not unitary. The Poletti declaration also demonstrates that the transfer function matrix relating to the sub-system path between "Omni" and S1-S4 is not unitary.

In view of the analyses and conclusions set forth in the Poletti declaration, it should now be clear that Jot et al. does not describe a system, or any sub-system, having a unitary transfer function matrix. Since Claim 1 expressly recites such a matrix as a feature of the claimed processor, it should be clear that Jot et al. does not anticipate the Applicant's claimed processor as set forth in Claim 1.

In view of the Poletti declaration and the foregoing remarks, it is believed that the rejection based on Section 102(e) is not supported by substantial evidence. Therefore, the rejection is improper and should be withdrawn.

The Applicant's claimed method as set forth in Claim 8 also includes the use of an early reflection generation stage having a unitary transfer function matrix. The same feature is also included in Claims 13 and 18. Therefore, Claims 8, 13, and 18 are novel relative to Jot et al. for at least the same reasons as Claim 1. Therefore, the rejection of those claims based on Section 102(e) as to those claims should also be withdrawn.

Claims 3-5 depend from Claim 1 either directly or indirectly and thus, include all of the features of Claim 1. Therefore, Claims 3-5 are allowable for at least the same reasons as Claim 1.

Claims 10-12 depend from Claim 8 either directly or indirectly and thus, include all of the features of Claim 8. Therefore, Claims 10-12 are allowable for at least the same reasons as Claim 8.

Claims 15-17 depend from Claim 13 either directly or indirectly and thus, include all of the features of Claim 13. Therefore, Claims 15-17 are allowable for at least the same reasons as Claim 13.

Claim 20 depends from Claim 18 and thus, includes all of the features of Claim 18. Therefore, Claim 20 is allowable for at least the same reasons as Claim 18.

Additional Remarks Relating to the Examiner's Responses to Applicant's Arguments

In paragraph 25 of the Official Action, the Examiner states that the processor outputs only two output signals and refers to Figure 1. The Examiner further states that it is unclear how the Applicant's invention differs from Jot et al. because the Applicant's claimed processor is configured to have a unitary transfer function. The Examiner notes that there are a number of delayed reproductions produced by the Applicant's processor, but the processor outputs only two output signals.

The Applicant respectfully disagrees with the Examiner's assertion that Figure 1 shows only two outputs for the processor. The processor actually outputs more than two signals, which is clearly shown in Figure 1 of the present application. As discussed above relative to the rejection based on lack of written description, the processor shown in Figure 1 outputs at least four signals. Each of the four signals is output to a speaker, speakers L_1 to L_k respectively. Figure 1 clearly shows a line extending from each speaker to the processor.

Applicant notes that the lines from the processor to speakers L_1 and L_3 are joined

near the processor for clarity, as are the lines to speakers L_2 and L_k. This does not mean that there are only two outputs from the processor. Co-joining of lines in a schematic diagram is just a technique used by those skilled in the art to simplify such diagrams.

Further, the number of output signals is not pertinent to the unitary transfer matrix feature of the Applicant's claimed processor.

In paragraph 26, the Examiner responds that the claims do not recite that the output is sent to the speakers. Claims 1 and 13 have been amended to recite that the processor has "...multiple outputs adapted for outputting delayed discrete reproductions of the microphone signals to a number of loud speakers placed to broadcast said delayed discrete reproductions of the microphone signals into the room or other space."

Claims 8 and 18 have also been amended to claim a processor having multiple outputs adapted for outputting signals to a number of loudspeakers and to recite the step of "...outputting the delayed discrete reproductions of the microphone signals for input to the number of loudspeakers to broadcast said delayed discrete reproductions of the microphone signals into the room or other space."

In view of the amendments to Claims 1, 8, 13, and 18, the Examiner's assertion is no longer valid and the Applicant's arguments are relevant. If the Examiner intends to maintain his contention despite the foregoing arguments and the Poletti declaration, then it is incumbent on the Examiner to come forward with technical reasons or authority to support such contention.

In paragraphs 27 to 33 of the Official Action, the Examiner refers to other arguments in the Applicant's previous response and allegedly responds to each of them. However, no new arguments are presented. The Examiner merely refers back to the comments presented in paragraph 25.

In paragraph 27, the Examiner disagrees with the Applicant's statement that in Jot et al., the "system outputs are generated such that the system output power gain is not constant with frequency because of the addition signal processing performed on the outputs of the delay line 731 and on the outputs of the unitary mixing matrix 741." As demonstrated in the Poletti declaration, the system described in Jot et al. does not have a unitary transfer function matrix such that the processor has an overall power gain that is substantially constant with the frequency to improve stability in the sound system. If the Examiner intends to maintain his contention despite the foregoing arguments and the Poletti declaration, then it is incumbent on the Examiner to come forward with technical reasons or authority to support such contention.

In paragraph 28, the Examiner disagrees with the Applicant's statement that in "the apparatus described in Jot et al. , the only output that might be sent to a loudspeaker or broadcast emanates from a subsystem (such as delays 731, 742 and matrix 741) that does not have a unitary transfer function matrix". As discussed above and demonstrated in the Poletti declaration, Jot et al. does not describe a system that has a unitary transfer function matrix. If the Examiner intends to maintain his contention despite the foregoing arguments and the Poletti declaration, then it is incumbent on the Examiner to come forward with technical reasons or authority to support such contention.

In paragraph 29, the Examiner disagrees with the Applicant's statement that "each of the outputs of the sound processing room module of Jot et al. are formed in a manner such that none of them meet the requirement of having a total power gain that is substantially constant with frequency to provide stability in the sound system". However, as discussed above and demonstrated in the Poletti declaration, Jot et al. does not describe a system that has a power gain that is substantially constant with frequency, because the Jot et al. system does not provide a unitary transfer function matrix. If the Examiner intends to maintain his contention despite the foregoing arguments and the Poletti declaration, then it is incumbent on the Examiner to come forward with technical reasons or authority to support such contention.

In paragraph 30, the Examiner disagrees with the Applicant's statement that "in considering the system in relation to outputs S1-S4, the section of the room module that generates those outputs does not have a unitary transfer function and the overall system producing those outputs does not have constant power gain with frequency to provide stability". As discussed above and demonstrated in the Poletti declaration, Jot et al. does not describe a system that has a unitary transfer function matrix. If the Examiner intends to maintain his contention despite the foregoing arguments and the Poletti declaration, then it is incumbent on the Examiner to come forward with technical reasons or authority to support such contention.

In paragraph 31, the Examiner disagrees with the Applicant's statement that "Jot et al. uses various components and combines them in a different manner than the applicant's claimed sound processor in order to simulate virtual sound sources. For example, the Jot et al. system adds reverberation to early reflections. Therefore, the resulting transfer function

is not unitary." As discussed above and demonstrated in the Poletti declaration, Jot et al. does not describe a system that has a unitary transfer function matrix. If the Examiner intends to maintain his contention despite the foregoing arguments and the Poletti declaration, then it is incumbent on the Examiner to come forward with technical reasons or authority to support such contention.

In paragraph 32, the Examiner disagrees with the Applicant's statement that "the overall transfer function matrix of the early reflection and reverberation sections [of Jot et al.] is not unitary to provide an overall power gain substantially constant with frequency." As discussed above and demonstrated in the Poletti declaration, Jot et al. does not describe a system that has a unitary transfer function matrix or that provides an overall power gain that is substantially constant with frequency. If the Examiner intends to maintain his contention despite the foregoing arguments and the Poletti declaration, then it is incumbent on the Examiner to come forward with technical reasons or authority to support such contention.

35 USC 103(a): Claims 6, 7, 16, and 17

The Examiner rejected Claims 6, 7, 16, and 17 under 35 USC 103(a) as being unpatentable over Jot et al. in view of WO 93/23847. As discussed in the previous response to this rejection, the Applicant submits that WO 93/23847 does not disclose the features of the Applicant's claimed system that are missing from Jot et al. Therefore, the proposed combination would not anticipate the Applicant's claimed system as set forth in Claims 6 and 7. Accordingly, it is believed that Claims 6 and 7 are allowable. Claims 16 and 17 are allowable for similar reasons.

In paragraph 33 of the Official Action mailed on July 26, 2006, the Examiner disagrees with the Applicant's argument, and refers to the "arguments above". Presumably, the arguments referred to are those set forth by the Examiner in paragraph 25 of the Official Action. No other arguments are presented by the Examiner in paragraphs 27 to 32. As discussed above with reference to the rejection of Claims 1, 8, 13, and 18, and demonstrated in the Poletti declaration, Jot et al. does not describe a system that has a unitary transfer function matrix or that provides an overall power gain that is substantially constant with frequency. WO 93/23847 does not describe or suggest the use of a unitary transfer function matrix that provides an overall power gain that is substantially constant with frequency as set forth in Claims 1 and 13. Claims 6 and 7 depend from Claim 1 either directly or indirectly, and thus include all of the features recited in that claim. Claims 16 and 17 depend from Claim 13 either directly or indirectly, and thus include all of the features recited in that claim. Therefore, the proposed combination of Jot et al. and WO 93/23847 does not result in a processor having all of the features claimed in Claim 6, Claim 7, Claim 16, or Claim 17. If the Examiner disagrees with the analysis presented in the Poletti declaration, then it is incumbent on the Examiner to come forward with technical reasons or authority to support such contention.

In the absence of a combination of references that would anticipate the Applicant's claimed processor as set forth in Claims 6, 7, 16, and 17 the rejection of those claims under Section 103(a) is not supported by substantial evidence. Accordingly, the rejection is improper and should be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, it is believed that this application is in condition for allowance. The Examiner is respectfully requested to reconsider the application in the light of the amendments and remarks presented hereinabove.

Respectfully submitted,

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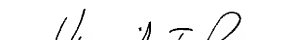

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